

Substitute for Form 1449/PTO			Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)			Application Number	10/613,006
			Filing Date	July 7, 2003
			First Named Inventor:	Scot A. Kellar
			Art Unit	2813
			Examiner Name	Dolan, Jennifer M.
			Attorney Docket Number	42P12750D
Sheet	1	of	3	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)		
JMS		EP	0293459 B1		Carlomagno et al.	

Examiner Signature		Date Considered	1/6/06
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<i>[Signature]</i>		US-	5,901,050	5/4/1999	Imai	
<i>[Signature]</i>		US-	6,391,669	5/21/2002	Fasano et al.	
<i>[Signature]</i>		US-	6,593,645	7/15/2003	Shih et al.	
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<i>[Signature]</i>		US-	6,882,045	4/19/2005	Massingill et al.	
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<i>[Signature]</i>		US-	US 2002/0017710 A1	2/14/2002	Kurashima et al.	
<i>[Signature]</i>		US-	US 2002/0195673 A1	12/26/2002	Chou et al.	
<i>[Signature]</i>		US-	US 2003/0148596 A1	8/7/2003	Kellar et al.	
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NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
		"Ultra Thin Electronics for Space Applications", 2001 Electronic Components and Technology Conference, 2001 IEEE, 5 pages.			
		"Copper Wafer Bonding"; A. Fan, A. Rahman, and R. Reif; Electrochemical and Solid-State Letters, 2 (10) 534-536 (1999).			
		"Face to Face Wafer Bonding for 3D Chip Stack Fabrication to Shorten Wire Lengths", Jun. 27-29, 2000 VMIC Conference 2000 IMIC-200/00/0090(c), 90-96.			
		"InterChip Via Technology for Vertical System Integration", Fraunhofer Institute for Reliability and Microintegration, Munich, Germany, Infineon Technologies AG, Munich, Germany, 2001 IEEE, 160-162.			

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